

FEATURES

- Dual Device Module
- Electrically Isolated Package
- Pressure Contact Construction
- International Standard Footprint
- Alumina (Non Toxic) Isolation Medium
- Integral Water Cooled Heatsink

APPLICATIONS

- Motor Control
- Controlled Rectifier Bridges
- Heater Control
- AC Phase Control

VOLTAGE RATINGS

Type Number	Repetitive Peak Voltages V_{DRM} V_{RRM} V	Conditions
MP04---590-18	1800	$T_{vj} = 0^{\circ}$ to $125^{\circ}C$, $I_{DRM} = I_{RRM} = 50mA$ $V_{DSM} = V_{RSM} =$ $V_{DRM} = V_{RRM} + 100V$ respectively
MP04---590-16	1600	
MP04---590-14	1400	

Lower voltage grades available.

ORDERING INFORMATION

Order As:

- MP04HBT590-18** or **MP04HBT-16** or **MP04HBT14**
MP04HBP590-18 or **MP04HBP-16** or **MP04HBP14**
MP04HBN590-18 or **MP04HBN-16** or **MP04HBN14**

Note: When ordering, please use the whole part number.

KEY PARAMETERS

V_{DRM}	1800V
$I_{T(AV)}$	595A
$I_{TSM(per\ arm)}$	16800A
V_{isol}	3000V

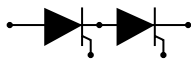
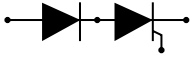
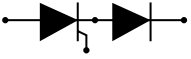
Code	Circuit
HBT	
HBP	
HBN	

Fig.1 Circuit diagrams

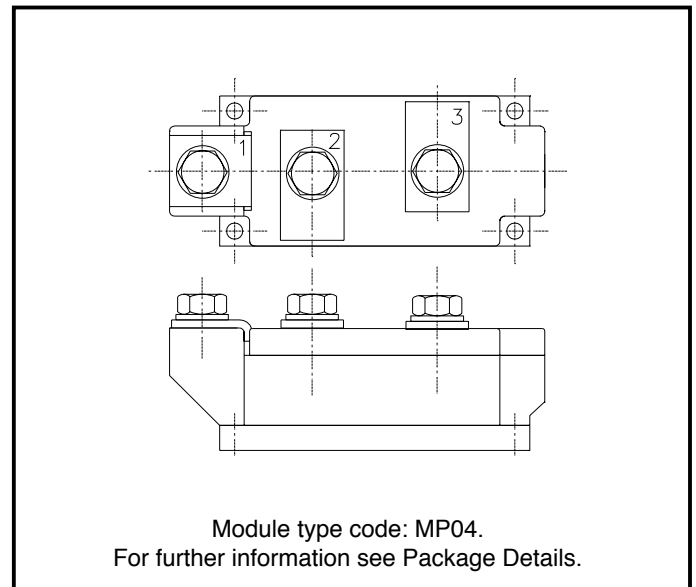


Fig. 2 Electrical connections - (not to scale)

ABSOLUTE MAXIMUM RATINGS - PER ARM

Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed. Exposure to Absolute Maximum Ratings may affect device reliability.

Symbol	Parameter	Test Conditions	Max.	Units	
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	$T_{case} = 75^{\circ}C$	595	A
			$T_{case} = 85^{\circ}C$	505	A
$I_{T(RMS)}$	RMS value	$T_{case} = 75^{\circ}C$	935	A	
I_{TSM}	Surge (non-repetitive) on-current	8.3ms half sine, $T_j = 125^{\circ}C$	16.8	kA	
I^2t	I^2t for fusing	$V_R = 0$	1411×10^3	A^2s	
I_{TSM}	Surge (non-repetitive) on-current	8.3ms half sine, $T_j = 125^{\circ}C$	13.5	kA	
I^2t	I^2t for fusing	$V_R = 50\% V_{DRM}$	911×10^3	A^2s	
I_{TSM}	Surge (non-repetitive) on-current	10ms half sine, $T_j = 125^{\circ}C$	15.7	kA	
I^2t	I^2t for fusing	$V_R = 0$	1232×10^3	A^2s	
I_{TSM}	Surge (non-repetitive) on-current	10ms half sine, $T_j = 125^{\circ}C$	12.6	kA	
I^2t	I^2t for fusing	$V_R = 50\% V_{DRM}$	794×10^3	A^2s	
V_{isol}	Isolation voltage	Commoned terminals to base plate. AC RMS, 1 min, 50Hz	3000	V	

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case (per thyristor or diode)	dc	-	0.056	°C/kW
		Half wave	-	0.060	°C/kW
		3 Phase	-	0.066	°C/kW
$R_{th(c-hs)}$	Thermal resistance - case to heatsink (per thyristor or diode)	Mounting torque = 5Nm with mounting compound	-	0.02	°C/kW
T_{vj}	Virtual junction temperature	Reverse (blocking)	-	125	°C
T_{stg}	Storage temperature range	-	-40	130	°C
-	Screw torque	Mounting - M6	-	6 (35)	Nm (lb.ins)
-		Electrical connections - M10	-	12 (106)	Nm (lb.ins)
-	Weight (nominal)	-	-	1580	g

DYNAMIC CHARACTERISTICS - THYRISTOR

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM} , $T_j = 125^\circ\text{C}$	-	50	mA
dV/dt	Linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125^\circ\text{C}$	-	1000	V/ μs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 1500A, gate source 1.5A, $t_r = 0.5\mu\text{s}$, $T_j = 125^\circ\text{C}$	-	500	A/ μs
$V_{T(TO)}$	Threshold voltage	At $T_{vj} = 125^\circ\text{C}$. See note 1	-	0.85	V
r_T	On-state slope resistance	At $T_{vj} = 125^\circ\text{C}$. See note 1	-	0.38	m Ω

Note 1: The data given in this datasheet with regard to forward voltage drop is for calculation of the power dissipation in the semiconductor elements only. Forward voltage drops measured at the power terminals of the module will be in excess of these figures due to the impedance of the busbar from the terminal to the semiconductor.

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	3.5	V
I_{GT}	Gate trigger current	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	200	mA
V_{GD}	Gate non-trigger voltage	At $V_{DRM}, T_{case} = 125^{\circ}C$	0.25	V
V_{FGM}	Peak forward gate voltage	Anode positive with respect to cathode	30	V
V_{FGN}	Peak forward gate voltage	Anode negative with respect to cathode	0.25	V
V_{RGM}	Peak reverse gate voltage	-	5	V
I_{FGM}	Peak forward gate current	Anode positive with respect to cathode	10	A
P_{GM}	Peak gate power	See table fig. 5	150	W
$P_{G(AV)}$	Mean gate power	-	10	W

CURVES

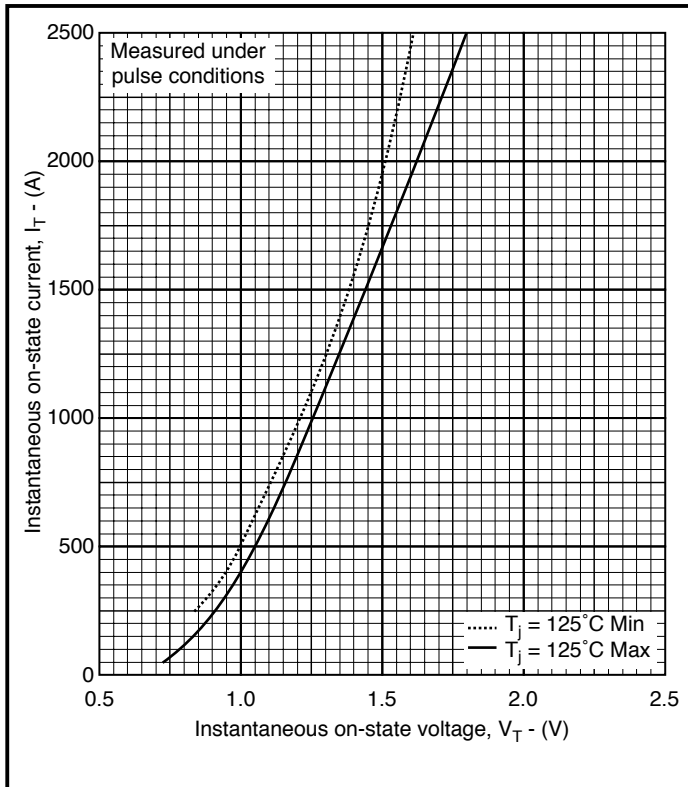


Fig. 3 Maximum (limit) on-state characteristics

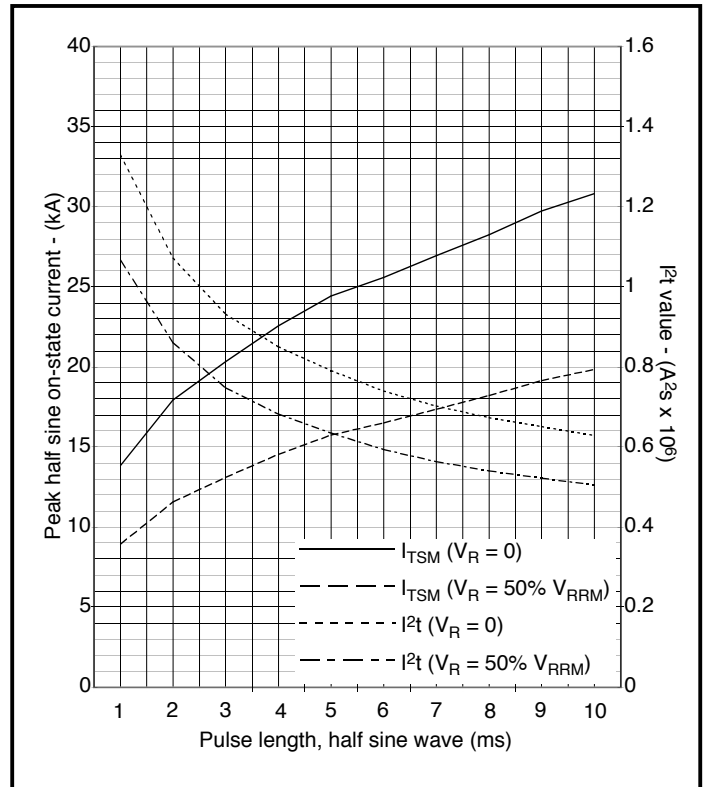


Fig. 4 Sub-cycle surge curves

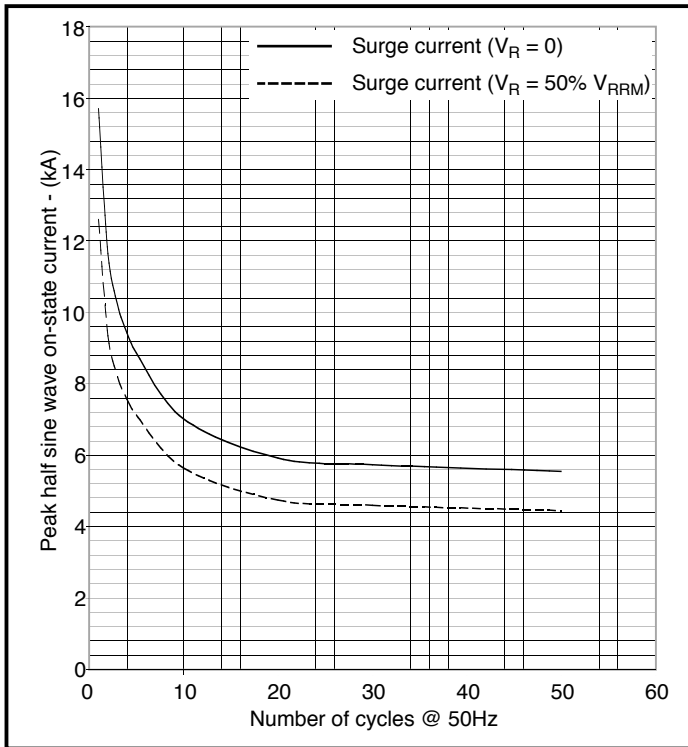


Fig. 5 Sub-cycle surge curves

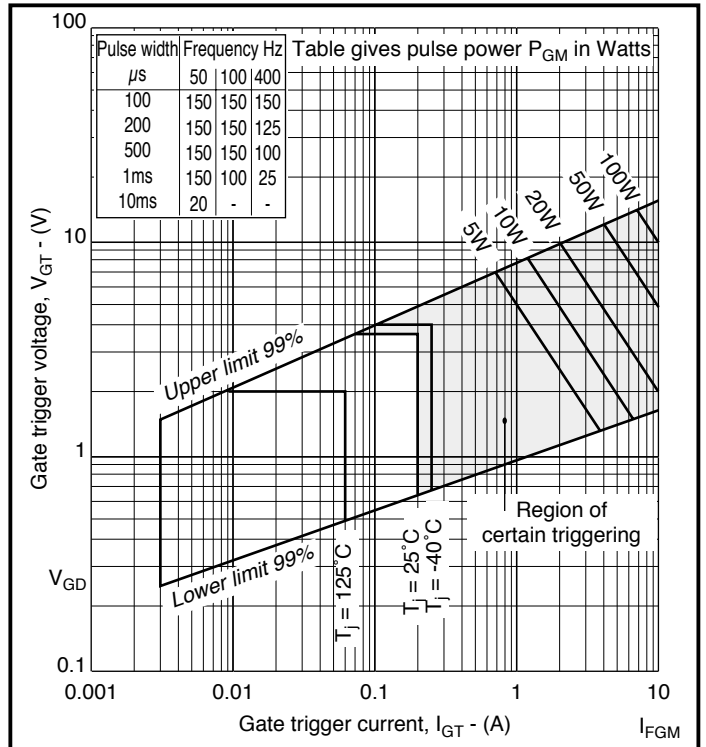


Fig. 6 Gate characteristics

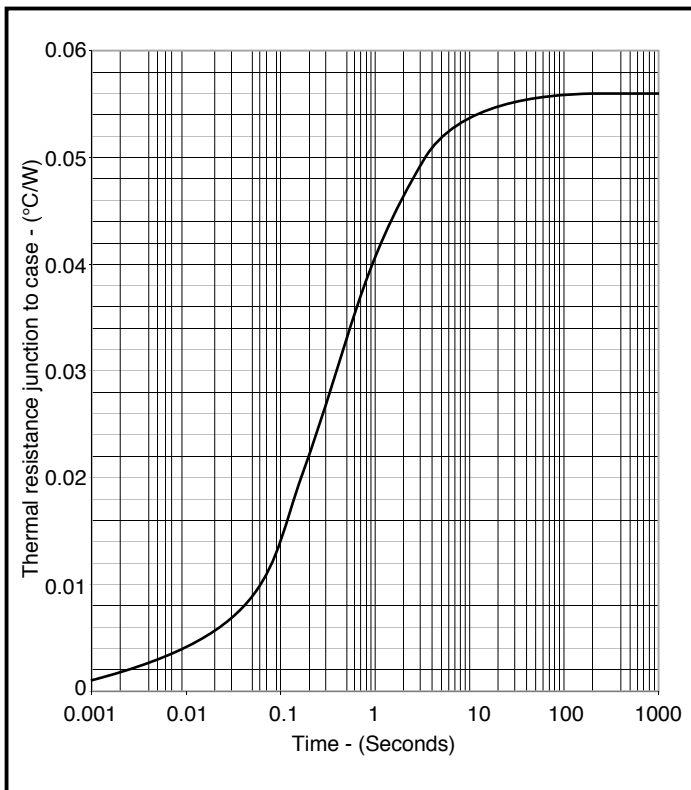


Fig. 7 Transient thermal impedance - dc

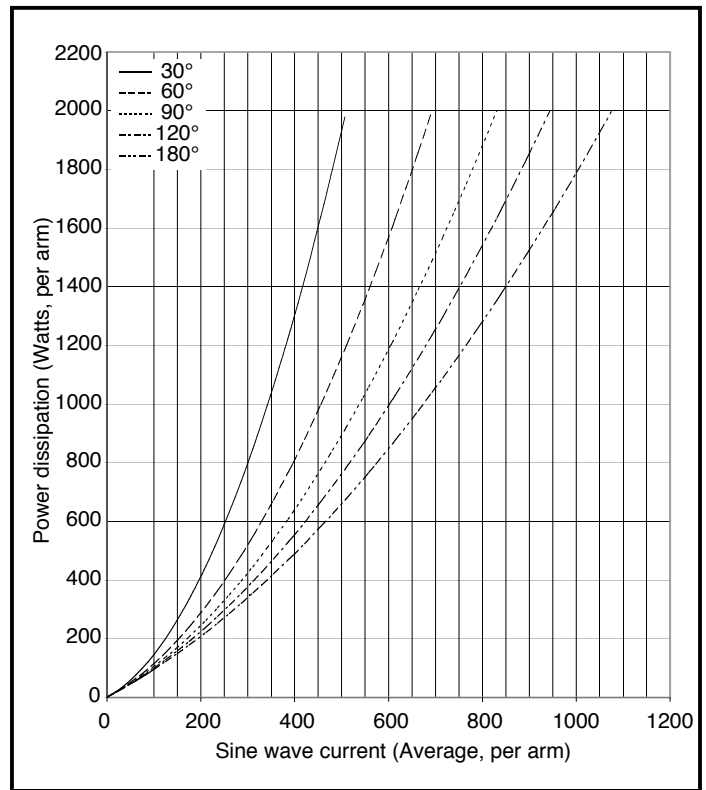


Fig. 8 On-state power loss per arm vs on-state current at specified conduction angles, sine wave 50/60Hz

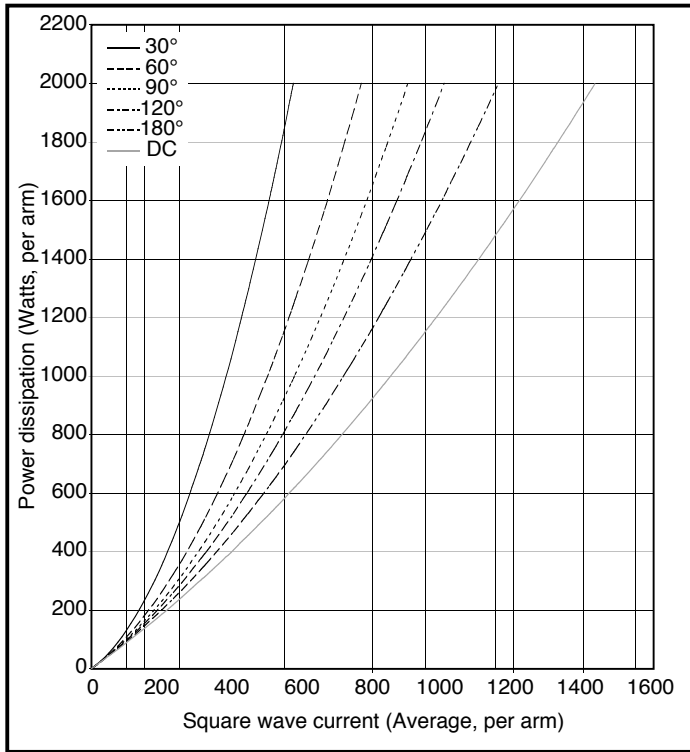


Fig. 8 On-state power loss per arm vs on-state current at specified conduction angles, square wave 50/60Hz

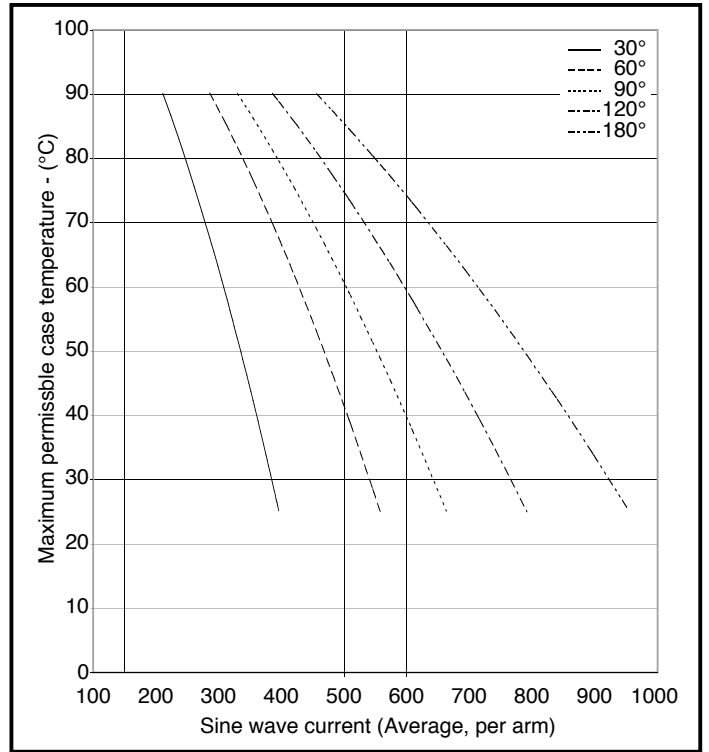


Fig. 9 Maximum permissible case temperature vs on-state current at specified conduction angles, sine wave 50/60Hz

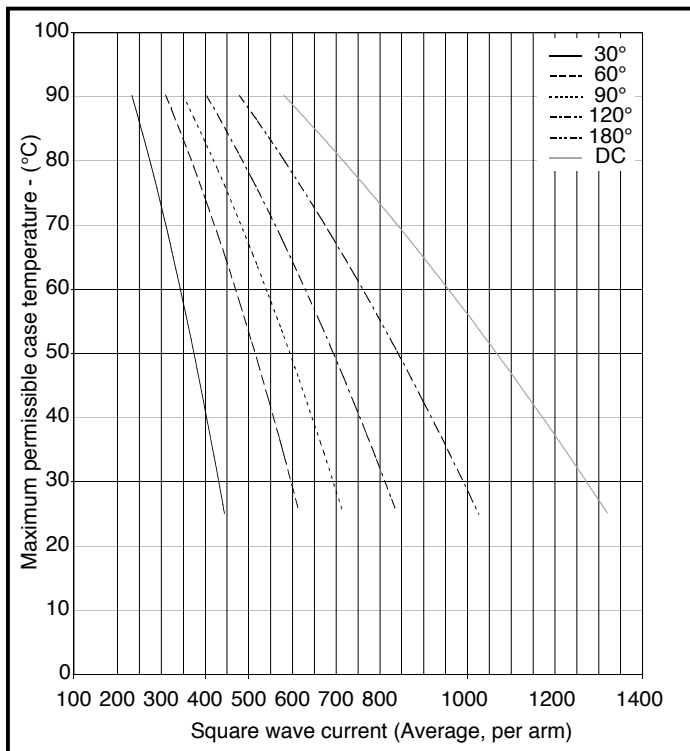


Fig. 10 Maximum permissible case temperature vs on-state current at specified conduction angles, square wave 50/60Hz

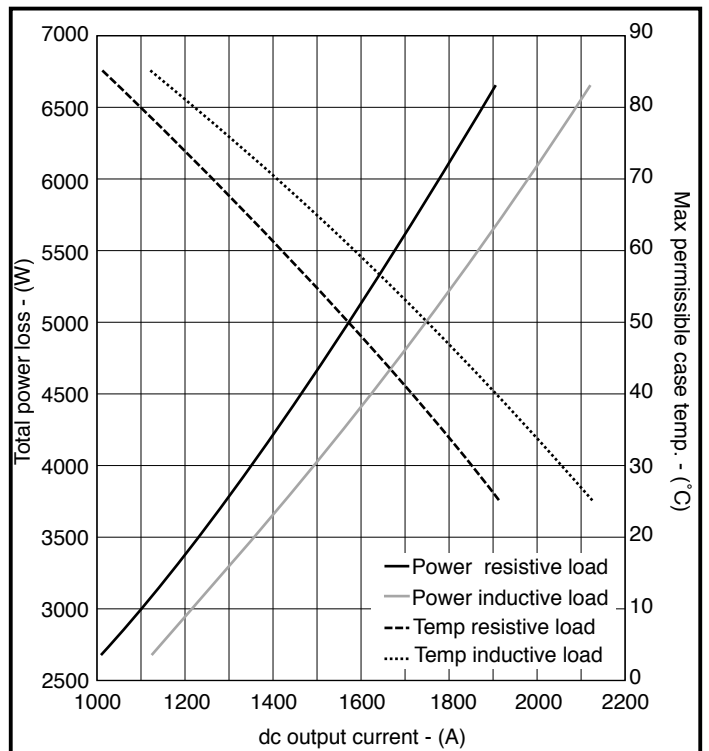


Fig. 11 50/60Hz single phase bridge DC output current vs power loss and maximum permissible case temperature

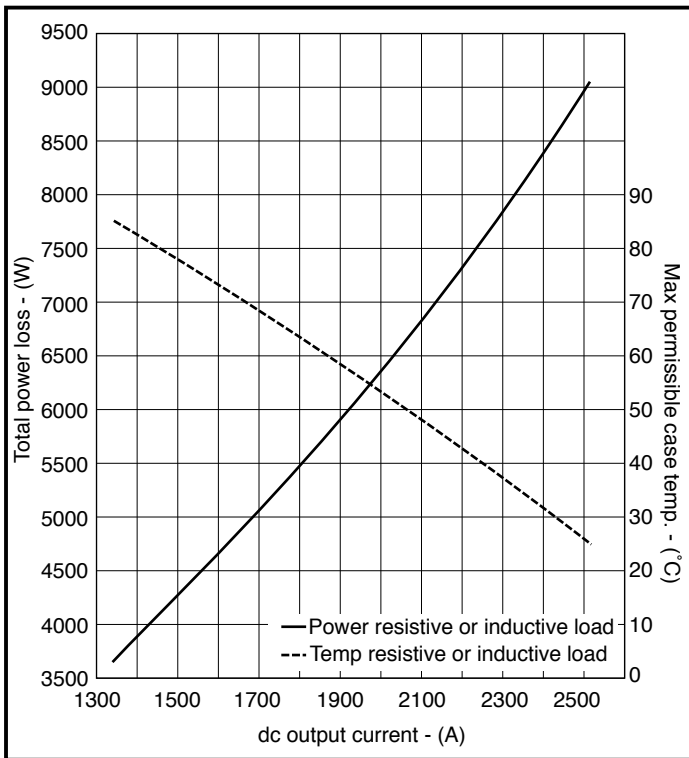
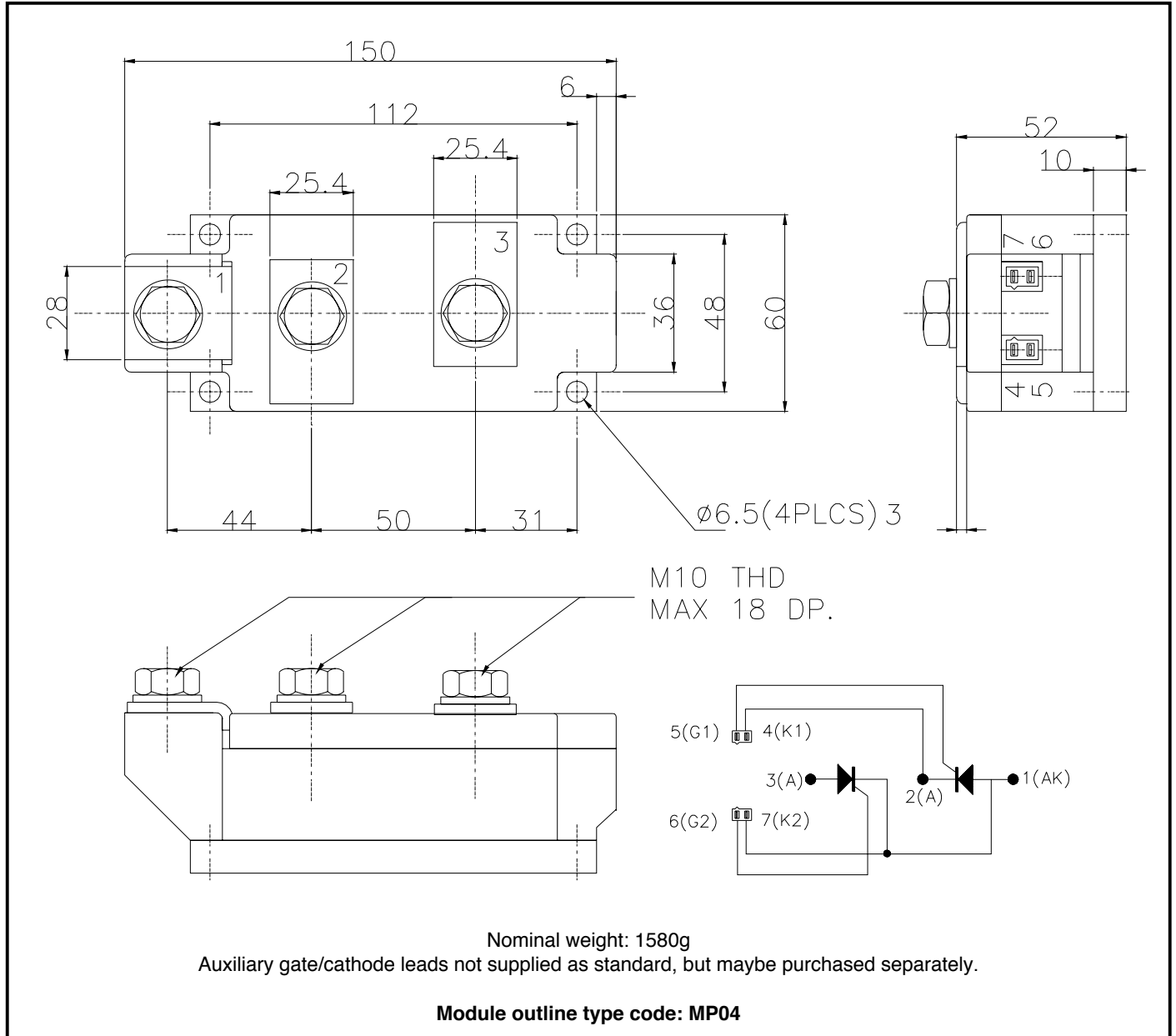


Fig. 12 50/60Hz Three phase bridge DC output current vs power loss and maximum permissible case temperature

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



MOUNTING RECOMMENDATIONS

Adequate heatsinking is required to maintain the base temperature at 75°C if full rated current is to be achieved. Power dissipation may be calculated by use of $V_{T(TO)}$ and r_T information in accordance with standard formulae. We can provide assistance with calculations or choice of heatsink if required.

The heatsink surface must be smooth and flat; a surface finish of N6 (32µin) and a flatness within 0.05mm (0.002") are recommended.

Immediately prior to mounting, the heatsink surface should be lightly scrubbed with fine emery, Scotch Brite or a mild chemical etchant and then cleaned with a solvent to remove oxide build up and foreign material. Care should be taken to ensure no foreign particles remain.

An even coating of thermal compound (eg. Unial) should be applied to both the heatsink and module mounting surfaces. This should ideally be 0.05mm (0.002") per surface to ensure optimum thermal performance.

After application of thermal compound, place the module squarely over the mounting holes, (or 'T' slots) in the heatsink. Fit and finger tighten the recommended fixing bolts at each end. Using a torque wrench, continue to tighten the fixing bolts by rotating each bolt in turn no more than 1/4 of a revolution at a time, until the required torque of 6Nm (55lbs.ins) is reached on all bolts at both ends.

It is not acceptable to fully tighten one fixing bolt before starting to tighten the others. Such action may DAMAGE the module.

POWER ASSEMBLY CAPABILITY

The Power Assembly group provides support for those customers requiring more than the basic semiconductor switch. Using CAD design tools the group has developed a flexible range of heatsink / clamping systems in line with advances in device types and the voltage and current capability of Dynex semiconductors.

An extensive range of air and liquid cooled assemblies is available covering the range of circuit designs in general use today.

HEATSINKS

The Power Assembly group has a proprietary range of extruded aluminium heatsinks. These were designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or customer service office.

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.



<http://www.dynexsemi.com>

e-mail: power_solutions@dynexsemi.com

HEADQUARTERS OPERATIONS
DYNEX SEMICONDUCTOR LTD
Doddington Road, Lincoln.
Lincolnshire. LN6 3LF. United Kingdom.
Tel: +44-(0)1522-500500
Fax: +44-(0)1522-500550

CUSTOMER SERVICE
Tel: +44 (0)1522 502753 / 502901. Fax: +44 (0)1522 500020

SALES OFFICES
Benelux, Italy & Switzerland: Tel: +33 (0)1 64 66 42 17. Fax: +33 (0)1 64 66 42 19.
France: Tel: +33 (0)2 47 55 75 52. Fax: +33 (0)2 47 55 75 59.
Germany, Northern Europe, Spain & Rest Of World: Tel: +44 (0)1522 502753 / 502901.
Fax: +44 (0)1522 500020
North America: Tel: (613) 723-7035. Fax: (613) 723-1518. Toll Free: 1.888.33.DYNEX (39639) /
Tel: (949) 733-3005. Fax: (949) 733-2986.

These offices are supported by Representatives and Distributors in many countries world-wide.
© Dynex Semiconductor 2002 TECHNICAL DOCUMENTATION – NOT FOR RESALE. PRODUCED IN UNITED KINGDOM

Datasheet Annotations:

Dynex Semiconductor annotate datasheets in the top right hand corner of the front page, to indicate product status. The annotations are as follows:-

Target Information: This is the most tentative form of information and represents a very preliminary specification. No actual design work on the product has been started.

Preliminary Information: The product is in design and development. The datasheet represents the product as it is understood but details may change.

Advance Information: The product design is complete and final characterisation for volume production is well in hand.

No Annotation: The product parameters are fixed and the product is available to datasheet specification.

This publication is issued to provide information only which (unless agreed by the Company in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. The Company reserves the right to alter without prior notice the specification, design or price of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to the Company's conditions of sale, which are available on request.

All brand names and product names used in this publication are trademarks, registered trademarks or trade names of their respective owners.